File 2:INSPEC 1969-2002/Mar W1

Set	Items	Description
S1	142799	TUNGSTEN OR W OR WOLFRAM
S2	336093	SILICON OR SI
S3	834	SILICON ON INSULATOR METAL OXIDE SEMICONDUCTOR OR SOI(W) MOSFET
S4	18195	CC=B2530F Metal-insulator-semiconductor structures
S5	495267	TRENCH?? OR HOLE? ? OR GROOVE? ? OR CHANNEL? ? OR EDGE? OR FLUSH OR RIDGE?
S6	63830	(EPI OR EPITAX?)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S7	89440	(INSULAT? OR DIELECTRIC OR OXIDE)(3N)(FILM? ? OR LAYER? OR COAT???? OR OVERCOAT???? OR MATERIAL? OR COVER???? OR MULTILAYER? OR MULTI(W)LAYER?)
S8	87875	GATE? ? OR MEMORY()CELL OR LIBRARY()CELL
S9	87	S3 AND S7
S10	77597	DRAIN? ? OR DRIFT? ? OR (ACTIVE OR DIFFUSION OR SOURCE)(2N)(REGION OR REGIONS OR AREAS OR AREA OR ZONE OR ZONES)
S11	35	S9 AND S10
S12	0	S11 AND S6
S13	26	S11 AND S5
S14	5	S3 AND (S1 AND S2)
S15	2252	(BURY??? OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?????)(3N)(INSULAT? OR DIELECTRIC OR OXIDE)
S16	101	S3 AND S15
S17	60	S16 AND S8
S18	44	S16 AND S10
S19	79	S17 OR S18
S20	44	S17 AND S5
S21	39	S18 AND S5
S22	12	S21 AND (METAL? OR POLYSILICON)
S23	14	S20 AND (METAL? OR POLYSILICON)
S24	17	S22 OR S23
S25	21	S13 NOT (S14 OR S22 OR S23)
S26	764	S3 AND (S1 OR S2)
S27	8	S3 AND S6
S28	7	S27 NOT (S25 OR S24 OR S14)
S29	95	S26 AND S15
S30	41	S29 AND S10
S31	23	S30 AND S8
S32	10	S31 NOT (S28 OR S25 OR S24 OR S14)
S33	4	S26 AND (METAL?)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S34	2	S33 NOT (S28 OR S25 OR S24 OR S14 OR S32)
S35	0	S26 AND (TUNGSTEN OR W OR WOLFRAM)(3N)(LAYER? OR FILM OR FILMS OR COAT????)
S36	6	S26 AND S6
S37	0	S36 NOT (S28 OR S25 OR S24 OR S14 OR S32 OR S34)

03/08/2002

? T S14/3,AB/1-5

14/3,AB/1
DIALOG(R)File 2:INSPEC

6111607 INSPEC Abstract Number: B9901-2560R-105, C9901-7410D-147
Title: A dynamic depletion **SOI MOSFET** model for SPICE
Author(s): Sinitsky, D.; Fung, S.; Tang, S.; Pin Su; Mansun Chan; Ping Ko ; Chenming Hu
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216) p.114-15
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xiii+227 pp.
ISBN: 0 7803 4770 6 Material Identity Number: XX98-01872
U.S. Copyright Clearance Center Code: 0 7803 4770 6/98/$10.00
Conference Title: 1998 Symposium on VLSI Technology Digest of Technical Papers
Conference Date: 9-11 June 1998 Conference Location: Honolulu, HI, USA
Language: English
Abstract: We show, using measurements, that a transition between partial and full depletion (PD and FD) modes of operation as terminal voltages vary with time (dynamic depletion) has a strong impact on thin film **SOI** **MOSFET** characteristics. A model incorporating this effect is presented. It includes floating body, backgate, and body contact nodes, as well as impact ionization, GIDL, diode leakage and parasitic bipolar currents. Self-heating is modeled by an auxiliary R/sub th/C/sub th/ circuit. The model uses a single smooth equation over all operating regimes for each current and charge and is fully scalable with T/sub **si**/, T/sub box/, T/sub ox/, **W**, and L.
Subfile: B C

14/3,AB/2
DIALOG(R)File 2:INSPEC

5909216 INSPEC Abstract Number: B9806-2560R-047
Title: Impact of scaling **silicon** film thickness and channel width on **SOI MOSFET** with reoxidized MESA isolation
Author(s): Fung, S.K.H.; Chan, M.; Ko, P.K.
Author Affiliation: Dept. of Electr. & Electron. Eng., Hong Kong Univ. of Sci. & Technol., Hong Kong
Journal: IEEE Transactions on Electron Devices vol.45, no.5 p. 1105-10
Publisher: IEEE,
Publication Date: May 1998 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(199805)45:5L.1105:ISSF;1-Y
Material Identity Number: I037-98005
U.S. Copyright Clearance Center Code: 0018-9383/98/$10.00
Language: English
Abstract: The characteristics of reoxidized MESA isolation for **silicon**-on-insulator (**SOI**) **MOSFET** have been studied in terms of the dependence of device performance on **silicon** film

thickness and channel width scaling. For devices with **silicon** film thickness (T/sub **Si**/) smaller than a critical thickness, humps appear in subthreshold IV and negative threshold voltage shift is observed in narrow width devices. The width encroachment (Delta **W**) also increases rapidly with reducing T/sub **Si**/. These observations can be explained by the formation of sharp beak and accelerated sidewall oxide growth in these devices. A simple guideline is given to optimize the reoxidation process for different T/sub **Si**/.
Subfile: B

14/3,AB/3
DIALOG(R)File 2:INSPEC

5835777 INSPEC Abstract Number: B9803-1265B-064, C9803-7410D-134
Title: Double gate dynamic threshold voltage (DGDT) SOI MOSFETs for low power high performance designs
Author(s): Liqiong Wei; Zhanping Chen; Roy, K.
Author Affiliation: Dept. of Electr. & Comput. Eng., Purdue Univ., West Lafayette, IN, USA
Conference Title: 1997 IEEE International SOI Conference Proceedings (Cat. No.97CH36069) p.82-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA xii+185 pp.
ISBN: 0 7803 3938 X Material Identity Number: XX97-03033
Conference Title: 1997 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 6-9 Oct. 1997 Conference Location: Fish Camp, CA, USA
Language: English
Abstract: In this paper, double gate dynamic threshold voltage (DGDT) SOI MOSFETs, which combine the advantages of DTMOS and FD SOI MOSFETs without the limitation of the supply voltage, are simulated using SOI-SPICE4.4. The threshold voltages, leakage currents and drive currents for FD SOI MOSFETs and DGDT SOI MOSFETs are compared. DGDT SOI MOSFETs show symmetric characteristics and the best I/sub on/I(off)/. Excellent DC inverter characteristics down to 0.15 V and good full adder performance at 1V are shown. The propagation delay and the average power consumption of the full adder are 0.625 ns and 11.5 mu **W**, respectively. It can be seen that DGDT **SOI MOSFET** is a good candidate for low power high performance designs.
Subfile: B C

14/3,AB/4
DIALOG(R)File 2:INSPEC

02862548 INSPEC Abstract Number: A87046312, B87023699
Title: Study of the laser-recrystallized film with a control of grain boundary location by using surrounding antireflection cap method
Author(s): Mukai, R.; Sasaki, N.; Nakano, M.
Author Affiliation: Div. of Adv. Technol., Fujitsu Ltd., Kawasaki, Japan
Journal: Journal of Electronic Materials vol.15, no.6 p.339-43
Publication Date: Nov. 1986 Country of Publication: USA
CODEN: JECMA5 ISSN: 0361-5235
Language: English

Abstract: A modified technique for unseeded laser-recrystallization of poly-crystalline **silicon** films deposited on amorphous insulators has been developed whereby grain boundary location in the recrystallized **silicon** film can be controlled. In this technique, the **silicon** film is encapsulated with an antireflection cap with windows and then recrystallized by CW-Ar ion laser irradiation. Grain boundaries are removed from the **silicon** film at the place where the window is opened because of the temperature gradient due to a change in laser-beam absorption in the **silicon** film. The (100) texture is observed in the grain-boundary-free areas although the **silicon** shows (110) texture before the recrystallization. An **SOI/MOSFET** has been fabricated in the recrystallized film. The channel regions of MOSFETs are aligned in the window regions. Field-effect mobility of 490 cm/sup 2//Vs is obtained for n-channel MOSFETs. Source-to-drain leakage current of 5 fA/ mu m is obtained at drain voltage of 5 V and back-gate voltage of -100 V for the W/L=10 mu m/2 mu m MOSFET.
Subfile: A B

14/3,AB/5
DIALOG(R)File 2:INSPEC

02519718 INSPEC Abstract Number: B85050780
Title: 3-dimensional integration fabricated by using seeded lateral epitaxial film on SiO/sub 2/
Author(s): Sasaki, N.; Iwai, T.; Kawamura, S.; Mukai, R.; Wada, K.; Nakano, M.
Author Affiliation: Div. of IC Dev., Fujitsu Ltd., Kasawaki, Japan
Conference Title: Comparison of Thin Film Transistor and SOI Technologies Symposium p.149-54
Editor(s): Lam, H.W.; Thompson, M.J.
Publisher: North-Holland, New York, NY, USA
Publication Date: 1984 Country of Publication: USA xv+321 pp.
ISBN: 0 444 00899 3
Conference Date: 26-28 Feb. 1984 Conference Location: Albuquerque, NM, USA
Language: English
Abstract: Seeded lateral epitaxial laser-recrystallization of **silicon** film on SiO/sub 2/ is applied to fabricate 3-dimensional (3-D) integrations: 3-D CMOS 7-stage ring oscillators. Top p-channel **Si**-gate SOI MOSFETs are fabricated in the seeded recrystallized **silicon** directly above bottom n-channel **Si**-gate bulk MOSFETs with an insulator in between. The recrystallized **silicon** at the seed region can be utilized for a buried contact to interconnect bottom and top MOSFETs. At the arsenic implantation step to fabricate source and drain of the bottom MOSFETs, ions are not implanted into the seed region to prevent heavy doping and crystal disorder there; otherwise the dopant diffuses laterally and residual crystal disorder disturbs the epitaxial recrystallization. After the laser-recrystallization, the seed region is implanted with phosphorus to interconnect the top and bottom MOSFETs. The Ar/sup +/ laser irradiation is performed with 10 **W** power, a 50 mu m spot size, a 13 cm/s scanning speed and a 13 mu m step at 400 degrees C in air. Propagation delay of 460 psec is obtained for the seven stage 3-D CMOS ring oscillator at a power supply voltage of 17 V for a channel length of 3 mu m and a channel width of 18 mu m. In the seeded SOI films, grain boundary generation and crystal orientation can be controlled.
Subfile: B

03/08/2002

? T S24/3,AB/1-5

24/3,AB/1
DIALOG(R)File 2:INSPEC

6882801 INSPEC Abstract Number: B2001-05-2560R-039
Title: Designing nanometre silicon-on-**insulator** MOSFET with **buried** Si/sub 1-x/Ge/sub x/ quantum well **channel**
Author(s): Fu, Y.; Patel, C.J.; Willander, M.
Author Affiliation: Dept. of Phys., Chalmers Univ. of Technol., Goteborg, Sweden
Journal: Physica E vol.9, no.4 p.694-700
Publisher: Elsevier,
Publication Date: April 2001 Country of Publication: Netherlands
CODEN: PELNFM ISSN: 1386-9477
SICI: 1386-9477(200104)9:4L.694:DNSI;1-C
Material Identity Number: G387-2001-004
U.S. Copyright Clearance Center Code: 1386-9477/2001/$20.00
Language: English
Abstract: We study the device characterization of Si-on-insulator (SOI) **metal** -oxide-semiconductor field effect transistor (MOSFET) with buried Si/sub 1-x/Ge, quantum well (QW) **channel**. Accurate quantum mechanical description of the p-**channel** of the buried Si/sub 1-x/Ge/sub x/ QW shows that the peak carrier concentration in the conduction **channel** is higher in the positively graded SiGe QW, whereas the carriers are more uniformly distributed in the retrograded QW. By phenomenologically introducing a physical parameter to describe the energy relaxation of the transmitting wave due to various scattering processes, systematic simulation about quantum wave transmission of our **SOI MOSFET** indicates normal current-bias characteristics in the nanometre regime. A threshold **gate** bias of about 0.6 V is obtained for both the positively graded and retrograded SiGe QWs.
Subfile: B

24/3,AB/2
DIALOG(R)File 2:INSPEC

6853009 INSPEC Abstract Number: B2001-04-2560R-031
Title: High performance **gate**-all-around devices using **metal** induced lateral crystallization
Author(s): Chan, V.W.C.; Chan, P.C.H.
Author Affiliation: Dept. of Electr. & Electron., Hong Kong Univ. of Sci. & Technol., China
Conference Title: 2000 IEEE International SOI Conference. Proceedings (Cat. No.00CH37125) p.112-13
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xi+143 pp.
ISBN: 0 7803 6389 2 Material Identity Number: XX-2000-02866
U.S. Copyright Clearance Center Code: 0 7803 6389 2/2000/$10.00
Conference Title: 2000 IEEE International SOI Conference. Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 2-5 Oct. 2000 Conference Location: Wakefield, MA, USA
Language: English
Abstract: Double **gate** or **gate**-all-around transistors were

predicted to continue the improvement in device performance down to 0.02 mu m **gate** length (Wong et al., 1997; Colinge et al., 1990; Tanaka et al., 1994). In this work, a high performance **gate** -all-around transistor (GAT) is demonstrated. The device is fabricated from either a bulk silicon wafer or on the top of any device layers. The fabrication process uses **metal** -induced-lateral-crystallization (MILC) to recrystallize the amorphous silicon to form large silicon grains in the **active area** . Using this technique, the transistor performance is comparable to a **SOI MOSFET** (Jagar et al., 1999). Compared to the method of cavity etch on the **buried oxide**, our method provides a uniform bottom **gate** length. Compared to the single-**gate** thin film transistor (SGT) and solid phase crystallization (SPC) devices, the GAT has lower subthreshold slope, lower threshold voltage, higher transconductance, nearly double the drive current and lower off-current. The impact of **channel** length and width scaling is investigated.

Subfile: B

24/3,AB/3

DIALOG(R)File 2:INSPEC

6852910 INSPEC Abstract Number: B2001-04-2560R-028

Title: A quasi-two dimensional model for fully depleted single **gate** SOI MOSFETS including temperature effects

Author(s): Gharabagi, R.

Author Affiliation: Dept. of Electr. Eng., St. Louis Univ., MO, USA

Conference Title: Proceedings of the IEEE 2000 National Aerospace and Electronics Conference. NAECON 2000. Engineering Tomorrow (Cat. No.00CH37093) p.508-15

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA xi+816 pp.

ISBN: 0 7803 6262 4 Material Identity Number: XX-2000-02759

U.S. Copyright Clearance Center Code: 0 7803 6262 4/2000/$10.00

Conference Title: Proceedings of the IEEE 2000 National Aerospace and Electronics Conference. NAECON 2000. Engineering Tomorrow

Conference Sponsor: Dayton Sect. IEEE; Aerosp. & Electron. Syst. Soc. (AESS) IEEE

Conference Date: 10-12 Oct. 2000 Conference Location: Dayton, OH, USA

Language: English

Abstract: A quasi-two dimensional model for single **gate** silicon on insulator (SOI) **Metal** Oxide Semiconductor Field Effect Transistors (MOSFETs) is presented. Major small geometry effects such as carrier velocity saturation, mobility degradation due to normal field, **channel** length modulation, and **drain** induced barrier lowering are included. The effects of parasitic bipolar transistor, impact ionization, and device self heating due to low thermal conductivity of **buried oxide** layer is also included. The device carrier mobility and threshold voltage are modeled as function of temperature. The effects of source, **drain**, and **channel** resistances are considered. Modeled results are then compared to measured data and are shown to be in good agreement over a wide range of operating voltages.

Subfile: B

24/3,AB/4

03/08/2002

DIALOG(R)File 2:INSPEC

6353067 INSPEC Abstract Number: B1999-10-2560R-079
Title: Transconductance oscillations in **metal**-oxide-semiconductor field-effect transistors with thin silicon-on-insulator originated by quantized energy levels
Author(s): Takahashi, T.; Miura-Mattausch, M.; Omura, Y.
Author Affiliation: Graduate Sch. of Adv. Sci. of Matter, Hiroshima Univ., Japan
Journal: Applied Physics Letters vol.75, no.10 p.1458-60
Publisher: AIP,
Publication Date: 6 Sept. 1999 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19990906)75:10L.1458:TOMO;1-9
Material Identity Number: A135-1999-035
U.S. Copyright Clearance Center Code: 0003-6951/99/75(10)/1458(3)/$15.00
Language: English
Abstract: Transconductance oscillations have been observed in silicon-on-insulator **metal** -oxide-semiconductor field-effect transistors with the separation by implanted oxygen technology at 39 K. Here, we demonstrate that the origin of the oscillations is attributed to a terrace structure of the **buried oxide** surface. The terrace results in different thicknesses of the active Si layer. Quantized energy levels at the thin Si layer are higher than those at the thicker one. These different energy levels act as barriers for carriers moving in the **channel** . The observed transconductance oscillations are well reproduced by fitting the effective terrace periodicity.
Subfile: B

24/3,AB/5
DIALOG(R)File 2:INSPEC

6284456 INSPEC Abstract Number: B1999-08-2560R-036
Title: High-performance accumulated back-interface dynamic threshold **SOI MOSFET** (AB-DTMOS) with large body effect at low supply voltage
Author(s): Takamiya, M.; Saraya, T.; Tran Ngoc Duyet; Yasuda, Y.; Hiramoto, T.
Author Affiliation: Inst. of Ind. Sci., Tokyo Univ., Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.38, no.4B p.2483-6
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: April 1999 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199904)38:4BL.2483:HPAB;1-H
Material Identity Number: F221-1999-010
Conference Title: Proceedings of the 1998 International Conference on Solid State Devices and Materials (SSDM'98)
Conference Date: 7-10 Sept. 1998 Conference Location: Hiroshima, Japan
Language: English
Abstract: A high-performance accumulated back-interface dynamic threshold silicon-on-insulator **metal** -oxide-semiconductor field effect transistor (AB-DTMOS) with a large body effect at low supply voltage (V/sub dd/<0.5 V) is proposed for low-power applications. In AB-DTMOS, the back

interface between the non-doped thin SOI and the **buried oxide** is accumulated by a large negative substrate bias, and the **gate** electrode is connected to this electrically induced body. AB-DTMOS realizes an ideal low/ultrahigh step **channel** profile electrically and achieves the maximum body effect. At fixed V/sub dd/, the body effect factor (gamma) of AB-DTMOS is twice as large as that of the conventional uniformly doped **channel** DTMOS, because the **channel** depletion layer width of AB-DTMOS is half that of the conventional DTMOS. Experimental results show a steep subthreshold slope, a high current drive due to a large V/sub dd/ shift, and a suppressed short **channel** effect.

Subfile: B

? T S24/3,AB/6-10

24/3,AB/6

DIALOG(R)File 2:INSPEC

6284414 INSPEC Abstract Number: B1999-08-2560R-033

Title: Buried layer engineering to reduce the **drain**-induced barrier lowering of sub-0.05 mu m **SOI-MOSFET**

Author(s): Koh, R.

Author Affiliation: Silicon Syst. Res. Labs., NEC Corp., Sagamihara, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.38, no.4B p.2294-9

Publisher: Publication Office, Japanese Journal Appl. Phys,

Publication Date: April 1999 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

SICI: 0021-4922(199904)38:4BL.2294:BLER;1-D

Material Identity Number: F221-1999-010

Conference Title: Proceedings of the 1998 International Conference on Solid State Devices and Materials (SSDM'98)

Conference Date: 7-10 Sept. 1998 Conference Location: Hiroshima, Japan

Language: English

Abstract: The influence of the buried layer structure on the **drain**-induced barrier lowering (DIBL) is investigated for a silicon-on-insulator **metal**-oxide-silicon field-effect-transistor (**SOI-MOSFET**) by a two-dimensional device simulator. The buried layer thickness and the **dielectric** constant of the **buried** layer are varied systematically. It is found that the degradation on the threshold voltage can be separated into two components. One component originates from the electric flux via the SOI layer and the other via the **buried** layer. The **buried insulator** engineering which controls the thickness and the **dielectric** constant of the **buried** layer is effective in reducing the latter component. The **gate** length limit can be reduced by 23% by the buried air gap structure where the **dielectric** constant of the **buried** layer is 1.0.

Subfile: B

24/3,AB/7

DIALOG(R)File 2:INSPEC

5909213 INSPEC Abstract Number: B9806-2560R-044

Title: **SOI MOSFET** with buried body strap by wafer bonding
Author(s): Kuehne, S.C.; Chan, A.B.Y.; Nguyen, C.T.; Wong, S.S.
Author Affiliation: Center for Integrated Syst., Stanford Univ., CA, USA
Journal: IEEE Transactions on Electron Devices vol.45, no.5 p. 1084-91
Publisher: IEEE,
Publication Date: May 1998 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(199805)45:5L.1084:MWBB;1-Y
Material Identity Number: I037-98005
U.S. Copyright Clearance Center Code: 0018-9383/98/$10.00
Language: English
Abstract: Although the **buried oxide** in the silicon-on-insulator (**SOI**) **MOSFET** makes possible higher performance circuits, it is also responsible for various floating body effects, including the kink effect, **drain** current transients, and history dependence of output characteristics. It is difficult to incorporate an effective contact to the body because of limitations imposed by the SOI structure. One candidate, which maintains device symmetry, is the lateral body contact. However, high lateral body resistance makes the contact effective only in narrow width devices. In this work, a buried lateral body contact in SOI is described which consists of a low-resistance **polysilicon** strap running under the MOSFET body along the device width. MOSFET's with effective **channel** length of 0.17 mu m have been fabricated incorporating this buried body strap, showing improved breakdown characteristics. Low leakage of the source and **drain** junctions demonstrates that the buried strap is compatible with deep submicron devices. Device modeling and analysis are used to quantify the effect of strap resistance on device performance. By accounting for the lateral resistance of the body, the model can be used to determine the maximum allowable device width, given the requirement of maintaining an adequate body contact.
Subfile: B

24/3,AB/8
DIALOG(R)File 2:INSPEC

5763184 INSPEC Abstract Number: B9801-2560R-031
Title: An analytical symmetric double-**gate** silicon-on-insulator **metal**-oxide-semiconductor field-effect-transistor model
Author(s): Sheng-Lyang Jang; Man-Chun Hu; Shau-Shen Liu
Author Affiliation: Nat. Taiwan Univ. of Sci. & Technol., Taipei, China
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.36, no.10 p.6250-3
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: Oct. 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199710)36:10L.6250:ASDG;1-G
Material Identity Number: F221-97019
Language: English
Abstract: A new complete and analytical **drain** current model for symmetric double-**gate** silicon-on-insulator **metal**-oxide-semicond uctor field-effect-transistors (SOI MOSFETs) is presented. The model applicable for digital/analog circuit simulation contains the following advanced features: precise description of the subthreshold, near threshold and above-threshold regions of operation by one single expression;

considering the source/**drain** resistance; inclusion of important short **channel** effects such as velocity saturation, **drain** induced barrier lowering and **channel** length modulation; self-heating effect due to the low thermal conductivity of the **buried oxide**; impact-ionization of MOS devices and parasitic bipolar junction transistor associated with **drain** breakdown. It was developed using a quasi-two-dimensional Poisson equation.
Subfile: B

24/3,AB/9
DIALOG(R)File 2:INSPEC

5611311 INSPEC Abstract Number: B9708-2560R-002
Title: An analytical fully-depleted silicon-on-insulator **metal**-oxide-semiconductor field-effect-transistor model considering the effects of self-heating, source/**drain** resistance, impact-ionization, and parasitic bipolar junction transistor
Author(s): Man-Chun Hu; Sheng-Lyang Jang; Young-Shying Chen; Shau-Shen Liu; Jien-Min Lin
Author Affiliation: Dept. of Electron. Eng., Nat. Taiwan Inst. of Technol., Taipei, Taiwan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.36, no.5A p.2606-13
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: May 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199705)36:5AL.2606:AFDS;1-M
Material Identity Number: F221-97010
Language: English
Abstract: This paper presents a simple, complete, and analytical **drain** current model for submicrometer silicon-on-insulator **metal**-oxide-semiconductor field-effect-transistor (**SOI MOSFET**). The model applicable for digital/analog circuit simulation contains the following advanced features: precise description of the subthreshold, near threshold, and above-threshold regions of operation by one single expression; precise description of I-V and G-V characteristics in the saturation region; single-piece **drain** current equation smoothly continuous from the linear region to saturation **region**; considering the **source/drain** resistance; inclusion of important short **channel** effects such as velocity saturation, **drain** induced barrier lowering and **channel** length modulation; self-heating effect due to the low thermal conductivity of the **buried oxide**; impact-ionization of MOS devices and the parasitic bipolar junction transistor (BJT) effect associated with **drain** breakdown. The model predicts that the parasitic resistances are important for submicron and deep submicron SOI MOS devices, the effects of impact-ionization and parasitic BJT are important in saturation region at small **gate** source voltage V(GF)/sub 1/ and self-heating effect is important in saturation region at large V/sub GF/. The present model agrees well with experimental results of various dimensions.
Subfile: B

24/3,AB/10
DIALOG(R)File 2:INSPEC

5484803 INSPEC Abstract Number: B9703-2560R-020
Title: Deep sub-micron **SOI MOSFET** with buried body strap
Author(s): Kuehne, S.C.; Chau, A.; Nguyen, C.T.; Wong, S.S.
Author Affiliation: Center for Integrated Syst., Stanford Univ., CA, USA
Conference Title: 1996 IEEE International SOI Conference Proceedings (Cat. No.35937) p.96-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA xvi+171 pp.
ISBN: 0 7803 3315 2 Material Identity Number: XX96-03123
Conference Title: 1996 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 30 Sept.-3 Oct. 1996 Conference Location: Sanibel Island, FL, USA
Language: English
Abstract: Reports on the implementation of a substrate contact in SOI consisting of a low resistance **polysilicon** strap within the **buried oxide** which contacts the SOI layer from the bottom. The efficacy of this buried strap is demonstrated in the grounded body **SOI MOSFET** . Various implementations of body contacts for SOI MOSFETs have been reported to alleviate problems associated with the floating body, such as the well-known kink and parasitic bipolar breakdown effects. The lateral body contact, which maintains device source/**drain** symmetry, has traditionally been limited in its effectiveness by the high resistance of the path that **holes** must travel laterally under the **gate** in order to reach the side contact. In this work, an effective lateral body contact, made possible by wafer bonding and etchback techniques, is demonstrated in deep sub-micron MOSFETs.
Subfile: B

? T S24/3,AB/11-13

24/3,AB/11
DIALOG(R)File 2:INSPEC

5336974 INSPEC Abstract Number: B9609-2560R-035
Title: **Buried-gate oxide** thinning during epitaxial lateral overgrowth for dual-**gated metal**-oxide-semiconductor field-effect transistors
Author(s): Watts, J.S.; Neudeck, G.W.
Author Affiliation: Sch. of Electr. & Comput. Eng., Purdue Univ., West Lafayette, IN, USA
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) vol.14, no.3 p.1670-4
Publisher: AIP for American Vacuum Soc,
Publication Date: May-June 1996 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(199605/06)14:3L.1670:BGOT;1-E
Material Identity Number: C067-96005
U.S. Copyright Clearance Center Code: 0734-211X/96/14(3)/1670/5/$10.00
Language: English
Abstract: During epitaxial lateral overgrowth of single-crystal silicon over thermal SiO/sub 2/, in the low-pressure chemical vapor deposition reactor environment, thinning and even pinholes can occur in the underlying **gate** oxide of in dual-**gated** silicon on insulator **metal**-oxide-semiconductor field-effect transistors (MOSFETs). The epitaxial

lateral overgrowth was grown using dichlorosilane (DCS), HCl, and H/sub 2/ at 970 degrees C and 40 Torr. Although the etch rate was very small, the thinning was large enough to change the bottom **channel** threshold voltage (Vt). Oxide thickness measurements, obtained by ellipsometry and by profilometer measurements, indicated an etch rate of about 0.1 nm/min, which was independently confirmed from MOSFET Vt shift measurements. The oxide etch rate decreased with increasing concentration of HCl and was less for oxides grown from heavily arsenic-doped than from lightly doped boron silicon.

Subfile: B

24/3,AB/12

DIALOG(R)File 2:INSPEC

5258289 INSPEC Abstract Number: B9606-2560R-092

Title: Comparison of standard and low-dose separation-by-implanted-oxygen substrates for 0.15 mu m **SOI MOSFET** applications

Author(s): Joachim, H.-O.; Yamaguchi, Y.; Fujino, T.; Kato, T.; Inoue, Y.; Hirao, T.

Author Affiliation: ULSI Lab., Mitsubishi Electr. Corp., Hyogo, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes (Japan) vol.35, no.2B p.983-7

Publisher: Publication Office, Japanese Journal Appl. Phys,

Publication Date: Feb. 1996 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

SICI: 0021-4922(199602)35:2BL.983:CSDS;1-J

Material Identity Number: C579-96005

Conference Title: 1995 International Conference on Solid State Devices and Materials (SSDM `95)

Conference Date: 21-24 Aug. 1995 Conference Location: Osaka, Japan

Language: English

Abstract: The influence of **buried oxide** thickness on short-**channel** effects in silicon-on-insulator **metal**-oxide-semiconductor field-effect transistors (SOI MOSFETs) is investigated. It is shown by analytical modeling and numerical simulation that, although a thin **buried oxide** helps to reduce the charge-sharing component of source and **drain** electric fields through the oxide layer, substrate depletion underneath the thin **buried oxide** counteracts the **oxide** thinning. Although this effect is desired below the **source** and **drain regions** to maintain the SOI inherent low junction capacitances, it is detrimental to short-**channel**-effect suppression. The calculated results are experimentally confirmed on 0.1 mu m **SOI MOSFET**`s fabricated on both standard and low-dose separation-by-implanted-oxygen (SIMOX) substrates. A new structure for 0.15 mu m **SOI MOSFET** applications on a thin **buried oxide** substrate is proposed in which substrate depletion below the **channel** -forming region can be suppressed locally using self-aligned deep ion implantation.

Subfile: B

24/3,AB/13

DIALOG(R)File 2:INSPEC

03/08/2002

5248793 INSPEC Abstract Number: B9606-2560R-011
Title: Fully depleted dual-**gated** thin-film SOI p-MOSFET with an isolated buried **polysilicon** backgate
Author(s): Denton, J.P.; Neudeck, G.W.
Author Affiliation: Sch. of Electr. Eng., Purdue Univ., West Lafayette, IN, USA
Conference Title: 1995 IEEE International SOI Conference Proceedings (Cat. No.95CH35763) p.135-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA xiv+183 pp.
ISBN: 0 7803 2547 8 Material Identity Number: XX95-02819
Conference Title: 1995 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron. Devices Soc
Conference Date: 3-5 Oct. 1995 Conference Location: Tucson, AZ, USA
Language: English
Abstract: A p-**channel** Dual-**Gated** Thin-Film Silicon-on-insulator (DG-TFSOI) MOSFET has been fabricated with an isolated buried **polysilicon** backgate and is in a SOI island. This structure allows individual operation of each backgate of each device, rather than the present common backgate (substrate) structure. The ability to use a individual buried **gate** to dynamically shift the threshold voltage of each individual top MOSFET may have significant implications for low power circuits and offers a way to boost drive currents for faster switching. By using Epitaxial Lateral Overgrowth (ELO) the bottom thermal **buried oxide** can be specified to any thickness.
Subfile: B

? T S24/3,AB/14-17

24/3,AB/14
DIALOG(R)File 2:INSPEC

5093323 INSPEC Abstract Number: B9512-1265D-013, C9512-5320G-006
Title: Design and performance of a new flash EEPROM on SOI(SIMOX) substrates
Author(s): Zaleski, A.; Ioannou, D.E.; Flandre, D.; Colinge, J.P.
Author Affiliation: Dept. of Electr. & Comput. Eng., George Mason Univ., Fairfax, VA, USA
Conference Title: 1994 IEEE International SOI Conference Proceedings (Cat. No.94CH35722) p.13-14
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xi+137 pp.
ISBN: 0 7803 2407 2
Conference Title: Proceedings of 1994 IEEE International SOI Conference
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 3-6 Oct. 1994 Conference Location: Nantucket, MA, USA
Language: English
Abstract: A new flash EEPROM cell and a novel erasing scheme on SOI substrates are reported. This flash EEPROM cell incorporates two separate control **gates**, located an opposite sides of the silicon film. One is a conventional control **gate** fabricated on top of the film as in bulk cells. The second control **gate** is the back **gate** itself, which is located underneath the silicon film and is inherent to all **SOI MOSFET** structures. As usual, the front control **gate** is used to WRITE the cell. By contrast, the back control **gate** is used to ERASE the cell in a new erasing scheme arrangement. In this scheme the back

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gate and the **drain** are used to invert the back **channel** and operate it in the impact ionization regime, such as to produce electron/**hole** pairs. Most of the generated electrons flow into the **drain** and some are injected into the back (**buried**) **oxide**. The **holes**, however, are accelerated towards the front **gate**, and many are finally injected into the floating **gate**, sandwiched between the front **gate** dioxide and front control **gate**. A prototype flash EEPROM cell was fabricated using a standard 1-**metal**, 1-poly CMOS SOI process and tested for concept proof. The cell was programmed via avalanche **channel** hot-electron injection from the **drain** pinch-off region, same as in bulk cells.

Subfile: B C

24/3,AB/15

DIALOG(R)File 2:INSPEC

4941833 INSPEC Abstract Number: B9506-2560R-017

Title: Two-dimensional analytical modeling of the source/**drain** engineering influence on short-**channel** effects in **SOI** **MOSFET**'s

Author(s): Joachim, H.-O.; Yamaguchi, Y.; Inoue, Y.; Tsvbouchi, N.

Author Affiliation: ULSI Lab., Mitsubishi Electr. Corp., Itami, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.34, no.2B p.822-6

Publication Date: Feb. 1995 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

Conference Title: 1994 International Conference on Solid State Devices and Materials (SSDM '94)

Conference Date: 23-26 Aug. 1994 Conference Location: Kanagawa, Japan

Language: English

Abstract: The scaling of the **metal**-oxide-semiconductor field-effect transistor (MOSFET) into the deep-submicron regime increases the influence of source/**drain** engineering, e.g., the use of a lightly doped source and **drain** (LDD) structure, on the transistor subthreshold characteristics due to the two-dimensional potential distribution. Device parameters like the subthreshold slope (S-factor) and the threshold voltage may become dependent on the LDD conditions. This paper presents a theoretical analysis of how source/**drain** conditions affect the short-**channel** behavior of fully depleted silicon-on-insulator (**SOI**) **MOSFET** 's. Accurate two-dimensional analytical modeling which takes into account the non-linear potential variation inside the **buried** **oxide** helps elucidate the mechanisms involved. The results, supported by numerical device simulation, indicate that for a correct description in addition to the different built-in potential of the source and **drain** junctions, an increasing effective **channel** length with LDD doping reduction must be taken into account.

Subfile: B

24/3,AB/16

DIALOG(R)File 2:INSPEC

04225007 INSPEC Abstract Number: B9210-2560R-013

Title: Thermal time constants in SOI-MOSFETs

03/08/2002

Author(s): Berger, M.; Burbach, G.
Author Affiliation: Dept. of Electron Devices & Circuits, Duisburg Univ., Germany
Conference Title: 1991 IEEE International SOI Conference Proceedings (Cat. No.91CH3053-6) p.24-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA xxii+183 pp.
ISBN: 0 7803 0184 6
U.S. Copyright Clearance Center Code: 0 7803 0184 6/91/$01.00
Conference Sponsor: IEEE
Conference Date: 1-3 Oct. 1991 Conference Location: Vail Valley, CO, USA
Language: English
Abstract: The authors present detailed theoretical considerations and a first-order analytical model for the dynamical behavior of self heating in SOIMOS (silicon-on-insulator **metal** oxide semiconductor). They show the results of the simulated spreading of heat when switching a SOIMOS in the on-state. At least four different time constants can be detected: spreading vertically through the **channel** region within about 100 ps; passing **gate** oxide and heating the polygate within 10 ns; heating up S/D-regions and **buried oxide** within 1 mu s; and at about 1 mu s heat energy reaches the substrate. The effects showing temperature rise vs. time in the **channel** and at backside interface are summarized. It is concluded that, in pulsed measurements of SOIMOS output characteristics, a pulse length of 10 ns will already produce an elevated temperature on the order of 10% of the steady-state value.
Subfile: B

24/3,AB/17
DIALOG(R)File 2:INSPEC

04038521 INSPEC Abstract Number: B9201-2560R-034
Title: Noise overshoot at **drain** current kink in **SOI MOSFET**
Author(s): Chen, J.; Fang, P.; Ko, P.K.; Hu, C.; Solomon, R.; Chan, T.-Y.; Sodini, C.G.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Conference Title: 1990 IEEE SOS/SOI Technology Conference. (Cat. No.90CH2891-0) p.40-1
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA vi+178 pp.
ISBN: 0 87942 573 3
U.S. Copyright Clearance Center Code: CH2891-0/90/0000-0040$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1990 Conference Location: Key West, FL, USA
Language: English
Abstract: The bias dependence of the **drain** current noise power of SOI (silicon-on-insulator) MOSFETs was studied, and low frequency noise overshoot at the **drain** current was observed. The overshoot has a width of about 0.7 V and exhibits a peak noise power which is two orders of magnitude higher than the normal noise level. The SOI devices used in this study were N-**channel polysilicon gate** MOSFETs on SIMOX (separation by implantation of oxygen) wafers fabricated with conventional submicron CMOS technology. The SOI film thickness, the **buried-oxide** thickness, and the **gate** oxide are 100 nm, 300 nm, and 11.5 nm, respectively. A computer-controlled test system was used to

conduct the I-V and noise measurement automatically. A model explaining the occurrence of the noise overshoot and the noise peak is proposed.

Subfile: B

? T S25/3,AB/1-5

25/3,AB/1
DIALOG(R)File 2:INSPEC

7097937 INSPEC Abstract Number: B2002-01-2560R-019
Title: Advanced **SOI** **MOSFET** 's with strained-Si/SiGe heterostructures
Author(s): Mizuno, T.; Sugiyama, N.; Kurobe, A.; Takagi, S.
Author Affiliation: Adv LSI Technol. Lab., Toshiba Corp., Yokohama, Japan
Journal: IEICE Transactions on Electronics Conference Title: IEICE Trans. Electron. (Japan) vol.E84-C, no.10 p.1423-30
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: Oct. 2001 Country of Publication: Japan
CODEN: IELEEJ ISSN: 0916-8524
SICI: 0916-8524(200110)E84C:10L.1423:AMWS;1-0
Material Identity Number: P712-2001-010
Conference Title: Joint Special Issue on Heterostructure Microelectronics with TWHM 2000 (Topical Workshop on heterostructure microelectronics 2000)
Conference Date: 20-23 Aug. 2000 Conference Location: Kyoto, Japan
Language: English
Abstract: We have developed advanced SOI n- and p-MOSFETs with strained-Si **channel** on insulator (strained SOI) structure fabricated by SIMOX (separation-by-implanted oxygen) technology. The characteristics of this strained-SOI substrate and electrical properties of strained-SOI MOSFETs have been experimentally studied. Using strained-Si/relaxed-SiGe epitaxy technology and the usual SIMOX process, we have successfully formed a layered structure of fully-strained-Si (20 nm)/fully relaxed-SiGe film (290 nm) on uniform buried **oxide layer** (85 nm) inside the SiGe layer. Good **drain** current characteristics have been obtained in strained-SOI MOSFETs. It is found that both electron and **hole** mobility is enhanced in strained-SOI MOSFETs, compared to the universal mobility in an inversion layer and the mobility of control SOI MOSFETs. These mobility enhancement factors are almost the same as the theoretical results.
Subfile: B

25/3,AB/2
DIALOG(R)File 2:INSPEC

6677752 INSPEC Abstract Number: B2000-09-2560R-127
Title: The ground-plane concept for the reduction of short-**channel** effects in fully-depleted SOI devices
Author(s): Ernst, T.; Cristoloveanu, S.
Author Affiliation: Lab. de Phys. des Composants a Semicond., ENSERG, Grenoble, France
Conference Title: Proceedings of the Ninth International Symposium on Silicon-on-Insulator Technology and Devices. (Electrochemical Society Proceedings Vol.99-3) p.329-34
Editor(s): Hemment, P.L.F.; Cristoloveanu, S.; Houston, T.W.; Izumi, K.; Hovel, H.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA x+374 pp.
ISBN: 1 56677 225 7 Material Identity Number: XX-2000-00258

Conference Title: Proceedings of Silicon-on Insulator Technology and Devices
Conference Sponsor: Electron. Soc
Conference Date: 2-7 May 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: The short-**channel** effects in sub-0.1 mu m fully-depleted **SOI MOSFET** devices involve not only charge sharing in the film but also fringing fields in the buried oxide and in the substrate. A possible solution, namely the use of a ground plane, is proposed, and compared to more conventional approaches. The influence of the source and **drain** coupling under the body on the subthreshold slope, back-**channel** conduction, **drain**-induced barrier lowering (DIBL) and charge sharing is simulated. The benefits of low resistance substrates and thin buried oxides are also examined.
Subfile: B

25/3,AB/3
DIALOG(R)File 2:INSPEC

6582531 INSPEC Abstract Number: B2000-06-2560R-033
Title: Buried oxide fringing capacitance: a new physical model and its implication on SOI device scaling and architecture
Author(s): Ernst, T.; Cristoloveanu, S.
Author Affiliation: Lab. de Phys. des Composants a Semicond., ENSERG, Grenoble, France
Conference Title: 1999 IEEE International SOI Conference. Proceedings (Cat. No.99CH36345) p.38-9
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA ix+138 pp.
ISBN: 0 7803 5456 7 Material Identity Number: XX-2000-00245
U.S. Copyright Clearance Center Code: 0 7803 5456 7/99/$10.00
Conference Title: 1999 IEEE International SOI Conference. Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 4-7 Oct. 1999 Conference Location: Rohnert Park, CA, USA
Language: English
Abstract: Fringing fields into the buried oxide and substrate depletion region stand as a key limiting factor for **SOI MOSFET** **channel** length reduction beyond 0.1 mu m. In fully-depleted (FD) SOI transistors, they cause a strong DIBL enhancement and a parasitic back **channel** conduction. On the other hand, in partially-depleted (PD) devices, the back **channel** control is even more difficult. The understanding and modeling of this phenomenon is of major interest, especially for RF SOI applications on high resistivity substrates where the depleted substrates behave as dielectrics. Various solutions to reduce these drawbacks are envisaged, such as buried oxide shrinking or double gate devices (Colinge, 1997; Cristoloveanu and Li, 1995). Thus far, the fringing field effect was ignored or merely included in FD analytical models by use of adjustable parameters. This paper presents a simple physical model for the evaluation of short **channel** effects induced by the BOX and substrate depletion. We analyze the lateral **drain** field penetration in the BOX and substrate, and calculate the related fringing capacitances. The model serves to anticipate the buried oxide scaling and substrate resistivity effects and to suggest the "ground plane" (GP) concept (Ernst and Cristoloveanu, 1999; Wong et al, 1998) as a suitable architecture for deep sub-micron SOI MOSFETs.

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Subfile: B

25/3,AB/4
DIALOG(R)File 2:INSPEC

6549639 INSPEC Abstract Number: B2000-05-2560R-049
Title: Monte Carlo simulation of conductance characteristics in **SOI-MOSFET**
Author(s): Araya, S.; Yamasaki, K.; Ueno, H.; Mori, N.; Hamaguchi, C.; Perron, L.M.; Lacaita, A.L.
Author Affiliation: Dept. of Electron. Eng., Osaka Univ., Japan
Journal: Physica B Conference Title: Physica B (Netherlands) vol.272, no.1-4 p.565-7
Publisher: Elsevier,
Publication Date: Dec. 1999 Country of Publication: Netherlands
CODEN: PHYBE3 ISSN: 0921-4526
SICI: 0921-4526(199912)272:1/4L.565:MCSC;1-G
Material Identity Number: M742-2000-002
U.S. Copyright Clearance Center Code: 0921-4526/99/$20.00
Conference Title: Eleventh International Conference on Nonequilibrium Carrier Dynamics in Semiconductors. HCIS-11
Conference Sponsor: IUPAP; Phys. Soc. Japan; Japan Soc. Appl. Phys.; IEEE Electron. Devices Soc. Tokyo
Conference Date: 19-23 July 1999 Conference Location: Kyoto, Japan
Language: English
Abstract: Front- and back-**channel** **drain** -conductance characteristics of SOI-MOSFETs are calculated by performing a Monte Carlo simulation, and the calculated results are compared with the experimental results of Perron et al. (Proceedings of the ESSDERC '98, 1998, p. 284) in order to extract the roughness parameters of the two interfaces. Effect of image charge in **oxide** **layers** in SOI structures is also discussed.
Subfile: B

25/3,AB/5
DIALOG(R)File 2:INSPEC

6540358 INSPEC Abstract Number: B2000-05-2560R-008
Title: The behavior of narrow-width SOI MOSFETs with MESA isolation
Author(s): Wang, H.; Chan, M.; Wang, Y.; Ko, P.K.
Author Affiliation: Inst. of Microelectron., Beijing Univ., China
Journal: IEEE Transactions on Electron Devices vol.47, no.3 p. 593-600
Publisher: IEEE,
Publication Date: March 2000 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(200003)47:3L.593:BNWM;1-0
Material Identity Number: I037-2000-003
U.S. Copyright Clearance Center Code: 0018-9383/2000/$10.00
Language: English
Abstract: Narrow-width effects in thin-**film** silicon on **insulator** (SOI) MOSFETs with MESA isolation technology have been studied theoretically and experimentally. As the **channel** width of the

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MOSFET is scaled down, the gate control of the **channel** potential is enhanced. It leads to the suppression of **drain** current dependence on substrate bias and punchthrough effect in narrow-width devices. The variation of threshold voltage with the **channel** width is also studied and is found to have a strong dependence on thickness of silicon film, interface charges in the buried oxide and **channel** type of SOI MOSFETs.
Subfile: B
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? T S25/3,AB/6-21

25/3,AB/6
DIALOG(R)File 2:INSPEC
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6479262 INSPEC Abstract Number: B2000-03-2560R-011
Title: An analytical model for fully depleted single gate SOI MOS transistors including lattice temperature effects
Author(s): Gharabagi, R.
Author Affiliation: Dept. of Electr. Eng., St. Louis Univ., MO, USA
Journal: International Journal of Electronics vol.87, no.2 p.129-36
Publisher: Taylor & Francis,
Publication Date: Feb. 2000 Country of Publication: UK
CODEN: IJELA2 ISSN: 0020-7217
SICI: 0020-7217(200002)87:2L.129:AMFD;1-U
Material Identity Number: I097-2000-002
Language: English
Abstract: An analytical model for fully depleted SOI MOSFETs is presented. Major small geometry effects such as carrier velocity saturation, mobility degradation, **channel** length modulation, and **drain** induced barrier lowering are included. Device self heating due to low thermal conductivity of a buried **oxide layer** is included in carrier mobility modelling. Thermal effects are also included in the threshold voltage expression. Source, **drain**, and **channel** resistance effects are also included. Modelled results are then compared to available measured data and are shown to be in very good agreement.
Subfile: B
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25/3,AB/7
DIALOG(R)File 2:INSPEC
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6379244 INSPEC Abstract Number: B1999-11-2560R-054
Title: Exploration of velocity overshoot in a high-performance deep sub-0.1- mu m **SOI MOSFET** with asymmetric **channel** profile
Author(s): Baohong Cheng; Rao, V.R.; Woo, J.C.S.
Author Affiliation: Adv. Products Res. & Dev. Lab., Motorola Inc., Austin, TX, USA
Journal: IEEE Electron Device Letters vol.20, no.10 p.538-40
Publisher: IEEE,
Publication Date: Oct. 1999 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199910)20:10L.538:EVOH;1-I
Material Identity Number: I338-1999-010
U.S. Copyright Clearance Center Code: 0741-3106/99/$10.00
Language: English

03/08/2002

Abstract: The electron velocity overshoot phenomenon in the inversion layer is experimentally investigated using a novel thin-**film** silicon-on-**insulator** (SOI) test structure with **channel** lengths down to 0.08 mu m. The uniformity of the carrier density and tangential field is realized by employing a lateral asymmetric **channel** (LAC) profile. The electron **drift** velocity observed in this work is 9.5*10/sup 6/ cm/s for a device with L/sub eff/=0.08 mu m at 300 K. The upward trend in electron velocity can be clearly noticed for decreasing **channel** lengths.
Subfile: B

25/3,AB/8
DIALOG(R)File 2:INSPEC

6262043 INSPEC Abstract Number: B1999-07-2560R-025
Title: A new structure design of a silicon-on-insulator MOSFET reducing the self-heating effect
Author(s): Awadallah, R.; Yuan, J.S.
Author Affiliation: Dept. of Electr. & Comput. Eng., Central Florida Univ., Orlando, FL, USA
Journal: International Journal of Electronics vol.86, no.6 p.707-12
Publisher: Taylor & Francis,
Publication Date: June 1999 Country of Publication: UK
CODEN: IJELA2 ISSN: 0020-7217
SICI: 0020-7217(199906)86:6L.707:SDSI;1-2
Material Identity Number: I097-1999-006
Language: English
Abstract: A new silicon-on-insulator (SOI) device structure is proposed. The new design provides a heat conducting path between the **channel** and substrate. The device has been verified in two-dimensional device simulation. This new structure reduces device self-heating and increases the **drain** current of the **SOI MOSFET**.
Subfile: B

25/3,AB/9
DIALOG(R)File 2:INSPEC

6112961 INSPEC Abstract Number: A9903-7340Q-001, B9902-2560R-001
Title: Hot-carrier effects in thin-film deep submicron **SOI/MOSFET**
Author(s): Cao Jianmin; Wu Chuanliang; Shen Wenzheng; Huang Chang
Author Affiliation: Xi'an Electron. Tech. Inst., Lintong, China
Journal: Chinese Journal of Semiconductors vol.19, no.4 p.280-6
Publisher: Science Press,
Publication Date: April 1998 Country of Publication: China
CODEN: PTTPDZ ISSN: 0253-4177
SICI: 0253-4177(199804)19:4L.280:CETF;1-6
Material Identity Number: A658-98028
Language: Chinese
Abstract: Starting with a 2D simulation of hot-carrier injection current, we have discussed the influence of different silicon **film** thickness, gate **oxide** thickness and substrate doping on the hot-carrier effects of thin-film deep submicron SOT/MOSFET. Simulation results indicate that

for different film thickness, the carrier concentration in front **channel** near the **drain** has different influence on the hot-carrier effects, sometimes the influence is decisive. Previous conflicting reports concerning SOI device hot-carrier effects may result from ignoring the influence of the carrier concentration on the hot-carrier effects. The simulation also indicates that there is a thickness range (60-100 nm), in which the hot-carrier effects is week and insensitive to the thickness. Furthermore, in this range, the hot-carrier effects is independent of gate oxide thickness and substrate doping. These is helpful to the design of high reliability thin-film submicron **SOI**/ **MOSFET**.

Subfile: A B

25/3,AB/10

DIALOG(R)File 2:INSPEC

5919495 INSPEC Abstract Number: B9806-2560R-077

Title: Source/**drain** engineering with Ge large angle tilt implantation and pre-amorphization to improve current drive and alleviate floating body effects of thin film SOI MOSFETs

Author(s): Hsiao, T.C.; Ping Liu; Lynch, W.T.; Woo, J.C.S.

Author Affiliation: Dept. of Electr. Eng., California Univ., Los Angeles, CA, USA

Conference Title: ESSDERC '97. Proceedings of the 27th European Solid-State Device Research Conference p.516-19

Editor(s): Grunbacher, H.

Publisher: Editions Frontieres, Paris, France

Publication Date: 1997 Country of Publication: France xvi+767 pp.

ISBN: 2 86332 221 4 Material Identity Number: XX97-02325

Conference Title: 27th European Solid-State Device Research Conference (ESSDERC '97)

Conference Date: 22-24 Sept. 1997 Conference Location: Stuttgart, Germany

Language: English

Abstract: This work presents an advanced salicide technology for thin **film** silicon-on-**insulator** (SOI) MOSFETs. Germanium large angle tilt implantation is applied to amorphize the silicon films prior to silicidation. This novel salicide technology greatly reduces the silicide formation energy and effectively controls the silicide depth. As a result source/**drain** parasitic resistances are substantially reduced. In addition, due to the formation of a metal-semiconductor barrier near the source/**channel** junction, the floating body effects are alleviated.

Subfile: B

25/3,AB/11

DIALOG(R)File 2:INSPEC

5598619 INSPEC Abstract Number: B9707-2560R-057

Title: 0.18- mu m fully-depleted silicon-on-insulator MOSFET's

Author(s): Min Cao; Kamins, T.; Voorde, P.V.; Diaz, C.; Greene, W.

Author Affiliation: Hewlett-Packard Labs., Palo Alto, CA, USA

Journal: IEEE Electron Device Letters vol.18, no.6 p.251-3

Publisher: IEEE,

03/08/2002

Publication Date: June 1997 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199706)18:6L.251:FDSI;1-B
Material Identity Number: I338-97006
U.S. Copyright Clearance Center Code: 0741-3106/97/$10.00
Language: English
Abstract: High-performance 0.18- mu m gate-length fully depleted silicon-on-insulator (FD-**SOI**) **MOSFET** 's were fabricated using 4-nm gate oxide, 35-nm thick **channel**, and 80-nm or 150-nm buried **oxide layer**. An elevated source/**drain** structure was used to provide extra silicon during silicide formation, resulting in low source/**drain** series resistance. Nominal device drive currents of 560 mu A/ mu m and 340 mu A/ mu m were achieved for n-**channel** and p-**channel** devices, respectively, at a supply voltage of 1.8 V. Improved short-**channel** performance and reduced self-heating were observed for devices with thinner buried **oxide layers**.
Subfile: B
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25/3,AB/12
DIALOG(R)File 2:INSPEC
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5523058 INSPEC Abstract Number: B9704-2560R-035
Title: Reduction of the reverse short **channel** effect in thick **SOI MOSFET**'s
Author(s): Tsoukalas, D.; Tsamis, C.; Kouvatsos, D.N.; Revva, P.; Tsoi, E.
Author Affiliation: Inst. of Microelectron., Aghia Paraskevi, Greece
Journal: IEEE Electron Device Letters vol.18, no.3 p.90-2
Publisher: IEEE,
Publication Date: March 1997 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(199703)18:3L.90:RRSC;1-Q
Material Identity Number: I338-97003
U.S. Copyright Clearance Center Code: 0741-3106/97/$10.00
Language: English
Abstract: We show that the reverse short **channel** effect (RSCE) is reduced in NMOS devices made in thick silicon-on-**insulator** (SOI) **material** . The reduction of the RSCE depends on the thickness of the Si overlayer. It is found that the thinner the Si film, the less the threshold voltage roll-on. The experimental findings are explained by a decrease of the lateral distribution of silicon interstitials generated at the source and **drain** (S/D) region and are related with their high recombination velocity at the buried oxide. This method can be used to separately test the influence of S/D point defects on the RSCE from other different hypotheses reported in the literature. Coupled process-device simulation reveals that the method is very sensitive to fundamental point defect properties.
Subfile: B
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DIALOG(R)File 2:INSPEC
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5368582 INSPEC Abstract Number: B9610-2560R-064

Title: Suppressing the parasitic bipolar action of ultra-thin **SOI MOSFET**'s using back-side-bias-temperature treatment
Author(s): Koizumi, H.; Shimaya, M.; Tsuchiya, T.
Author Affiliation: NTT LSI Labs., Atsugi, Japan
Conference Title: 1996 IEEE International Reliability Physics Proceedings. 34th Annual (Cat. No.96CH38525) p.27-32
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA vi+396 pp.
ISBN: 0 7803 2753 5 Material Identity Number: XX96-01074
U.S. Copyright Clearance Center Code: 0 7803 2753 5/96/$5.00
Conference Title: Proceedings of International Reliability Physics Symposium
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Reliability Soc
Conference Date: 30 April-2 May 1996 Conference Location: Dallas, TX, USA
Language: English
Abstract: A new suppression method for parasitic bipolar action is presented for fully depleted surface-**channel** nMOSFET's on SOI by using the back-side-bias-temperature (BSBT) treatment technique. This method improves subthreshold characteristics, source-**drain** breakdown voltage, and hot-carrier instability without degrading device characteristics. BSBT treatment can suppress the parasitic bipolar action regardless of stress bias polarity. BSBT damage to the back-side interface between buried **oxide** and active silicon **layer** was investigated using several methods. The suppression mechanism proposed is the generation of fixed charges and interface traps at the back-side interface.
Subfile: B

25/3,AB/14
DIALOG(R)File 2:INSPEC

5093338 INSPEC Abstract Number: B9512-2560R-037
Title: Series resistance at metal contact for thin film **SOI MOSFET**
Author(s): Chang-Bong Oh; Jonghyon Ahn; Sucheon Lee; Young-Wug Kim; Donghyun Kim; Bonggi Kim
Author Affiliation: Samsung Semicond., San Jose, CA, USA
Conference Title: 1994 IEEE International SOI Conference Proceedings (Cat. No.94CH35722) p.43-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA xi+137 pp.
ISBN: 0 7803 2407 2
Conference Title: Proceedings of 1994 IEEE International SOI Conference
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 3-6 Oct. 1994 Conference Location: Nantucket, MA, USA
Language: English
Abstract: Thin-**film** silicon-on-**insulator** (TFSOI) MOSFET has emerged as a strong candidate for high performance, high density and latch-up free CMOS devices with less fabrication steps. Thin silicon film should be used to achieve good behavior in **SOI MOSFET**. However, most of the papers on TFSOI have reported high parasitic source/**drain** series resistance and contact resistance, which tends to obscure the performance advantages of SOI. In this paper, we examined effects of top silicon film thickness (Tsi) on contact series resistance and contact **hole** etching method.
Subfile: B

25/3,AB/15
DIALOG(R)File 2:INSPEC

4907169 INSPEC Abstract Number: B9505-2560R-006
Title: Scaling constraints imposed by self-heating in submicron **SOI MOSFET**'s
Author(s): Dallmann, D.A.; Shenai, K.
Author Affiliation: Dept. of Electr. & Comput. Eng., Wisconsin Univ., Madison, WI, USA
Journal: IEEE Transactions on Electron Devices vol.42, no.3 p. 489-96
Publication Date: March 1995 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/95/$04.00
Language: English
Abstract: The presence of a buried **oxide layer** in silicon causes enhanced self-heating in Silicon-On-Insulator (SOI) n-**channel** MOSFETs. The self-heating becomes more pronounced as device dimensions are reduced into the submicron regime because of increased electric field density and reduced silicon volume available for heat removal. Two-dimensional numerical simulations are used to show that self-heating manifests itself in the form of degraded drive current due to mobility reduction and premature breakdown. The heat flow equation was consistently solved with the classical semiconductor equations to study the effect of power dissipation on carrier transport. The simulated temperature increases in the **channel** region are shown to be in close agreement with recently measured data. Numerical simulation results also demonstrated accelerated turn-on of the parasitic bipolar transistor due to self-heating. Simulation results were used to identify scaling constraints caused by the parasitic bipolar transistor turn-on effect in SOI CMOS ULSI. For a quarter-micron n-**channel SOI MOSFET** , results suggest a maximum power supply of 1.8 V. In the deep submicron regime, SOI devices exhibited a negative differential resistance due to increased self-heating with **drain** bias voltage. Detailed comparison with bulk devices suggested significant reduction in the **drain**-source avalanche breakdown voltage due to increased carrier injection at the source-body junction.
Subfile: B

25/3,AB/16
DIALOG(R)File 2:INSPEC

4669270 INSPEC Abstract Number: B9406-2560R-082
Title: Modeling of **edge** threshold voltage of mesa-isolated n-**channel** MOSFETs on fully-depleted thin film SOI
Author(s): Jae-Woo Park; Chul-Hi Han; Choong-Ki Kim
Author Affiliation: Dept. of Electron. Eng., Kum-Oh Nat. Univ. of Technol., Kyungbuk, South Korea
Journal: Solid-State Electronics vol.37, no.7 p.1449-52
Publication Date: July 1994 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
U.S. Copyright Clearance Center Code: 0038-1101/94/$6.00+0.00

03/08/2002

Language: English
Abstract: In silicon-on-insulator (SOI) technology, the non-**active** **regions** can be eliminated by thorough etch-out of the Si film, which results in the mesa-shaped Si **film** islands on the **insulator** and each device is fabricated on these individual islands. Therefore, the lateral isolation between devices is nearly ideal, but the island **edge** effects are inevitable. Higher positive fixed charge on the sidewalls along with low doping can lead to a smaller turn-on voltage for the parasitic sidewall MOSFETs compared with the front **channel** MOSFET. The early turn-on of the sidewall transistor shows up as a hump in the subthreshold characteristics of the whole device and can result in excessive subthreshold leakage. Although several investigations about the **edge** effects of **SOI MOSFET** have been reported, they are confined only to the physical analyses for the **edge** effects, and, moreover, the **edge** threshold voltage model is given only for the case of partially depleted thick film SOI MOSFETs. In this paper, we study the **edge** effects of mesa-isolated, fully-depleted, n-**channel** MOSFETs fabricated on thin film SOI and suggest an analytical **edge** threshold voltage model.
Subfile: B

25/3,AB/17
DIALOG(R)File 2:INSPEC
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04367884 INSPEC Abstract Number: B9304-2560R-079
Title: Floating-body effect free concave SOI-MOSFETs (COSMOS)
Author(s): Hieda, K.; Takedai, S.; Takahashi, M.; Yoshimi, M.; Takato, H.; Nitayama, A.; Horiguchi, F.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: International Electron Devices Meeting 1991. Technical Digest (Cat. No.91CH3075-9) p.667-70
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA 977 pp.
ISBN: 0 7803 0243 5
U.S. Copyright Clearance Center Code: CH3075-9/91/0000-0667$1.00
Conference Sponsor: IEEE
Conference Date: 8-11 Dec. 1991 Conference Location: Washington, DC, USA
Language: English
Abstract: In order to overcome the degradation induced by floating body effects and to suppress the increase in parasitic source/**drain** resistances in thin-**film** silicon-on-**insulator** (SOI) MOSFETs, a concave **SOI-MOSFET** (COSMOS) is proposed. This structure realizes a partially thin-film SOI region, which is used as a fully depleted **channel**, and thick-film SOI regions, which are used as source/**drain**. The unique features of the COSMOS are found to be (1) elimination of the floating-body effects, (2) less short **channel** effect, (3) excellent subthreshold characteristics, and (4) reduction in parasitic source/**drain** resistances.
Subfile: B

25/3,AB/18
DIALOG(R)File 2:INSPEC
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04261630 INSPEC Abstract Number: B9212-1265D-003

Title: Low-power and high-stability SRAM technology using a laser-recrystallized p-**channel SOI MOSFET**
Author(s): Takao, Y.; Shimada, H.; Suzuki, N.; Matsukawa, Y.; Sasaki, N.
Author Affiliation: Fujitsu Ltd., Kawasaki, Japan
Journal: IEEE Transactions on Electron Devices vol.39, no.9 p. 2147-52
Publication Date: Sept. 1992 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/92/$03.00
Language: English
Abstract: Laser recrystallization of p-**channel** SOI MOSFETs on an undulated **insulating layer** is demonstrated for SRAMs with low power and high stability. Self-aligned p-**channel** SOI MOSFETs for loads are stacked over bottom n-**channel** bulk MOSFETs for both drivers and transfer gates. A sufficient laser power assures the same leakage currents between SOI MOSFETs fabricated on an undulated **insulating layer** in memory cell regions and on an even **insulating layer** in field regions. The on/off ratio of the SOI MOSFETs is increased by a factor of 10/sup 4/, and the source-**drain** leakage current is decreased by a factor of 10-10/sup 2/ compared with those of polysilicon thin-film transistors (TFTs) fabricated by using low-temperature regrowth of amorphous silicon. A test 256-kb SRAM fabricated this technology shows improved stand-by power dissipation and cell stability. The process steps can be decreased to 83% of those TFT load SRAMs if both the peripheral circuit and memory cells are made with p-**channel** SOI and n-**channel** bulk MOSFETs.
Subfile: B

25/3,AB/19
DIALOG(R)File 2:INSPEC

04175790 INSPEC Abstract Number: B9208-2560R-003
Title: Single-transistor-latch-induced degradation of front- and back-**channel** thin-film SOI transistors
Author(s): Zhang, B.; Yoshino, A.; Ma, Tso-Ping
Author Affiliation: Dept. of Electr. Eng., Yale Univ., New Haven, CT, USA
Journal: IEEE Electron Device Letters vol.13, no.5 p.282-4
Publication Date: May 1992 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/92/$03.00
Language: English
Abstract: The front- and back-**channel** transistor characteristics in thin-**film** silicon-on-**insulator** (SOI) MOSFETs have been studied before and after front-**channel** hot-carrier stress resulting from single-transistor latch. This stress causes the following significant changes: (a) a reduction of the front-**channel** current for a given gate voltage, (b) an increase in front-**channel drain**-source breakdown voltage when measured in the reverse mode, and (c) a decrease in the back-**channel** transconductance. These changes can be attributed to the hot-carrier induced interface traps on both front and back interfaces near the **drain** junction.
Subfile: B

25/3,AB/20
DIALOG(R)File 2:INSPEC

03332031 INSPEC Abstract Number: B89023601
Title: Transconductance enhancement mechanisms in ultra-thin (<or=1000 AA) silicon-on-insulator MOSFETs
Author(s): Sturm, J.C.; Tokunaga, K.; Colinge, J.-P.
Author Affiliation: Dept. of Electr. Eng., Princeton Univ., NJ, USA
Journal: IEEE Transactions on Electron Devices vol.35, no.12 p. 2431-2
Publication Date: Dec. 1988 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/88/1200-2431$01.00
Conference Title: 46th Annual Device Research Conference
Conference Sponsor: IEEE
Conference Date: 20-22 June 1988 Conference Location: Boulder, CO, USA
Language: English
Abstract: Two advantages of ultrathin (<or=1000 AA) silicon-on-**insulator** (SOI) **films** for MOSFETs that have not previously been reported are described. Compared to bulk FETs of similar dimensions are doping levels, the effects have been observed to give up to 35% increase in **drain** saturation current or transconductance. Both experimental data and modeling are discussed. It is noted that the kink effect is absent in the ultrathin-film SOI FETs, and that the results were adjusted to account for the difference in threshold voltage in the n-**channel** bulk and ultrathin-film structures. In general, an increase in saturation current should lead to faster circuits. The experiments and modeling results to date are for long-**channel** structures only.
Subfile: B

25/3,AB/21
DIALOG(R)File 2:INSPEC

02519297 INSPEC Abstract Number: B85050594
Title: Transient analysis of **drain** current in silicon-on-insulator (SOI) MOSFETs
Author(s): Kato, K.; Wada, T.; Taniguchi, K.
Author Affiliation: VLSI Res. Center, Toshiba Corp., Kawasaki, Japan
Conference Title: Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials p.68-9 supl
Publisher: Business Centre for Acad. Sci. Japan, Tokyo, Japan
Publication Date: 1984 Country of Publication: Japan 2 vol. (ix+721+xix+88) pp.
ISBN: 4 930813 07 7
Conference Sponsor: Japan Soc. Appl. Phys.; IEEE; Electrochem. Soc. Japan ; et al
Conference Date: 30 Aug.-1 Sept. 1984 Conference Location: Kobe, Japan
Language: English
Abstract: A MOSFET having **channel** length of 2 mu m is fabricated on an SOI substrate in a standard process line. Gate **oxide** and SOI **film** thicknesses are 70 nm and 1 mu m, respectively. The turn-on **drain** current overshoots by up to more than twice the steady-state value, and then decreases to a steady-state value in about 200 mu sec. The authors developed a rigorous 2-carrier and transient SOI device simulator to analyze the switching characteristics.
Subfile: B

? T S28/3,AB/1-7

28/3,AB/1
DIALOG(R)File 2:INSPEC

6943576 INSPEC Abstract Number: B2001-07-2560R-031
Title: Fabrication and properties of ultra-short gate length ultra-thin **SOI MOSFET**'s
Author(s): Suzuki, E.; Ishii, K.; Kanemaru, S.
Author Affiliation: Electrotech. Lab., Ibaraki, Japan
Conference Title: 4th European Workshop on Low Temperature Electronics. WOLTE-4 p.43-7
Publisher: Eur. Space Agency, Noordwijk, Netherlands
Publication Date: 1999 Country of Publication: Netherlands 356 pp.
Material Identity Number: XX-2000-01436
Conference Title: Proceedings of Fourth Workshop on Low Temperature Electronics (WOLTE4)
Conference Date: 21-23 June 2000 Conference Location: Noordwijk, Netherlands
Language: English
Abstract: Ultra-short gate length ultra-thin SOI n-MOSFETs using some kinds of SOI wafers have been fabricated and their properties have been investigated. High suppression of the short-channel effect (SCE), e.g. V/sub th/ roll-off and S-slope degradation, is experimentally shown in the 40-135-nm gate length regime of ultra-thin SOI n-MOSFET's fabricated by using an SOI wafer prepared by the **epitaxial layer** transfer technique. The effectiveness of the ultra-thin SOI layer in preventing the SCE is systematically confirmed. It is also shown that the uniformity and lower roughness of the ultra-thin SOI layer are important for device operation, especially low temperature operation.
Subfile: B

28/3,AB/2
DIALOG(R)File 2:INSPEC

6695921 INSPEC Abstract Number: A2000-20-8115N-001, B2000-10-0520X-008
Title: Growth of epitaxial CoSi/sub 2/ for contacts of ultra-thin SOI MOSFETs
Author(s): Sakamoto, K.; Maeda, T.; Hasegawa, M.
Author Affiliation: Electrotech. Lab., Tsukuba, Japan
Journal: Thin Solid Films Conference Title: Thin Solid Films (Switzerland) vol.369, no.1-2 p.240-3
Publisher: Elsevier,
Publication Date: 3 July 2000 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(20000703)369:1/2L.240:GECC;1-K
Material Identity Number: T070-2000-017
U.S. Copyright Clearance Center Code: 0040-6090/2000/$20.00
Conference Title: International Joint Conference on Silicon Epitaxy and Heterostructures (IJC-Si)
Conference Date: 12-17 Sept. 1999 Conference Location: Miyagi, Japan
Language: English
Abstract: Epitaxial CoSi/sub 2/ growth for source/drain contacts of a ultra-thin silicon on insulator (**SOI**) **MOSFET** is discussed. In

order to attain low series resistance, heavily doped Si diffusion layer should be left undepleted under the grown CoSi/sub 2/. Contact resistance between epitaxial CoSi/sub 2/ and n/sup +/Si(001) increases when less than 1 nm Co is deposited. A salicide compatible process, forming a thin epitaxial CoSi/sub 2/ template by oxide mediated epitaxy followed by reaction deposition epitaxy to increase thickness, is effective in growing CoSi/sub 2/ epitaxially up to a few tens of nm.
Subfile: A B

28/3,AB/3
DIALOG(R)File 2:INSPEC

5886111 INSPEC Abstract Number: B9805-2560R-053
Title: Full-band Monte Carlo investigation of hot carrier trends in the scaling of metal-oxide-semiconductor field-effect transistors
Author(s): Duncan, A.; Ravaioli, U.; Jakumeit, J.
Author Affiliation: Illinois Univ., Urbana, IL, USA
Journal: IEEE Transactions on Electron Devices vol.45, no.4 p. 867-76
Publisher: IEEE,
Publication Date: April 1998 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(199804)45:4L.867:FBMC;1-Z
Material Identity Number: I037-98004
U.S. Copyright Clearance Center Code: 0018-9383/98/$10.00
Language: English
Abstract: A full-band Monte Carlo (MC) device simulator has been used to study the effects of device scaling on hot electrons in different types of n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) structures. Simulated devices include a conventional MOSFET with a single source/drain implant, a lightly-doped drain (LDD) MOSFET, a silicon-on-insulator (**SOI**) **MOSFET**, and a MOSFET built on an **epitaxial layer** on top of a heavily-doped ground plane. Different scaling techniques have been applied to the devices, to analyze the effects on the electric field and on the energy distributions of the electrons, as well as on drain, substrate, and gate currents. The results provide a physical basis for understanding the overall behavior of impact ionization and gate oxide injection and how they relate to scaling. The observed nonlocality of transport phenomena and the nontrivial relationship between electric fields and transport parameters indicate that simpler models cannot adequately predict hot carrier behavior at the channel lengths studied (sub-0.3- mu m). In addition, our results suggest that below 0.15 mu m, the established device configurations (e.g. LDD) that are successful at suppressing the hot carrier population for longer channel lengths, become less useful and their cost-effectiveness for future circuit applications needs to be reevaluated.
Subfile: B

28/3,AB/4
DIALOG(R)File 2:INSPEC

5484799 INSPEC Abstract Number: B9703-2560R-018
Title: Thin-film SOI p-MOSFET from epitaxial lateral overgrowth (ELO) with

a 200 AA nitrided SiO/sub 2/ backgate and large Delta V/sub T,top/ Vs V/sub G,back/ for ultra low power
Author(s): Chang, J.C.; Denton, J.P.; Neudeck, G.W.
Author Affiliation: Sch. of Electr. & Comput. Eng., Purdue Univ., West Lafayette, IN, USA
Conference Title: 1996 IEEE International SOI Conference Proceedings (Cat. No.35937) p.88-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA xvi+171 pp.
ISBN: 0 7803 3315 2 Material Identity Number: XX96-03123
Conference Title: 1996 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 30 Sept.-3 Oct. 1996 Conference Location: Sanibel Island, FL, USA
Language: English
Abstract: To achieve faster circuits with increased circuit density and reduced power, fully depleted (FD) dual-gated (DG) thin-film SOI-MOSFETs with an isolated buried backgate have been fabricated by using epitaxial lateral overgrowth (ELO) into SOI islands. Situated in an SOI island the fully depleted DG **SOI MOSFET** allows independent operation of both topgate and backgate, which is buried and totally isolated from all other devices. This provides a method to control the threshold voltage change of the top MOSFET with a bias on the backgate for fully-depleted devices. For example, the backgate can switch the top MOSFET to more `on' for larger drive currents and to more `off' for lower subthreshold leakage currents.
Subfile: B

28/3,AB/5
DIALOG(R)File 2:INSPEC

04016667 INSPEC Abstract Number: B91077142
Title: An analytical model for snapback in n-channel **SOI MOSFET**'s
Author(s): Huang, J.S.T.; Kueng, J.S.; Fabian, T.
Author Affiliation: Honeywell Inc., Plymouth, MN, USA
Journal: IEEE Transactions on Electron Devices vol.38, no.9 p. 2082-91
Publication Date: Sept. 1991 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/91/0900-2082$01.00
Language: English
Abstract: An analytical snapback model for n-channel silicon-on-insulator (SOI) transistors with body either tied to the source or floating is been presented. The snapback is modeled as a nonlinear feedback system leading to negative transconductances from which the jump in current can occur at the point of instability. The crux of this model is based on the strong dependence of the transistor threshold voltage on the body potential when the body potential is above the transistor surface potential at strong inversion. No parasitic bipolar action is invoked to account for the snapback phenomena. The model correctly predicts the occurrence of hysteresis/latch phenomena and the conditions under which the current jump occurs despite some gross approximations in the electric field and the injection level. Results obtained from this model show good agreement with experimental data measured from SIMOX devices fabricated on 0.3- mu m **epi film**.

Subfile: B

28/3,AB/6
DIALOG(R)File 2:INSPEC

02594267 INSPEC Abstract Number: B86009163
Title: Deep depleted SOI MOSFETs with back potential control: a numerical simulation
Author(s): Balestra, F.; Brini, J.; Gentil, P.
Author Affiliation: Lab. de Phys. des Composants a Semicond., ERA-CNRS, ENSERG, Grenoble, France
Journal: Solid-State Electronics vol.28, no.10 p.1031-7
Publication Date: Oct. 1985 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
U.S. Copyright Clearance Center Code: 0038-1101/85$3.00+.00
Language: English
Abstract: The authors consider **SOI MOSFET** structures (N and P type) for which control of the back potential of the **epi layer** is obtained by using a back gate. The effect of interface parameters on the back and front threshold voltages is analysed in the case of a strong coupling between front and back interface (lightly doped **epi layer**). This analysis is carried out by a numerical integration of Poisson's equation throughout the structure. The authors thus obtain the potential profile and the electron and hole densities, as a function of the applied front (V/sub g1/) and back (V/sub g2/) gate voltages. They also derive the I/sub d/(V/sub g1/,V/sub g2/) characteristics in the case of low drain voltage. This program allows them to examine the dependence of both front and back threshold voltages on the interfacial parameters. It is also used to examine the validity of the existing analytical models and to interpret experimental results obtained on MOS/SOS transistors.
Subfile: B

28/3,AB/7
DIALOG(R)File 2:INSPEC

02479279 INSPEC Abstract Number: B85040770
Title: Simulation of deep depleted SOI MOSFETs with back potential control
Author(s): Balestra, F.; Brini, J.; Gentil, P.
Author Affiliation: Lab. de Phys. des Composants a Semiconducteurs, ENSERG, Grenoble, France
Journal: Physica B & C vol.129B+C, no.1-3 p.296-300
Publication Date: March 1985 Country of Publication: Netherlands
CODEN: PHBCDQ ISSN: 0378-4363
U.S. Copyright Clearance Center Code: 0378-4363/85/$03.30
Conference Title: Proceedings of the 14th European Solid State Device Research Conference, including Solid State Device Technology
Conference Date: 10-13 Sept. 1984 Conference Location: Lille, France
Language: English
Abstract: The authors consider **SOI MOSFET** structures of N and P types for which a control of the back potential of the **epi layer** is obtained by using a back gate. The action of the interface parameters on the back and front threshold voltages is analysed in the case of a strong coupling between the front and back interface (lightly doped **epi layer**). This analysis is carried out by a numerical simulation of Poisson's equation throughout the structure. They thus obtain

the potential profile and the electron and hole densities, as a function of front (V/sub g1/) and back (V/sub g2/) gate voltages. They also deduce the I/sub d/(V/sub g1/,V/sub g2/) characteristics in the case of low drain voltage. Experimental material is given by CMOS/SOS transistors, the sapphire substrate of which has been locally thinned down. Comparison of the experimental I/sub d/(V/sub g2/) characteristics with the simulated characteristics allows the authors to determine directly the fast state density and the fixed charge at the back interface.

03/08/2002

T S32/3,AB/1-10

32/3,AB/1
DIALOG(R)File 2:INSPEC

7169975 INSPEC Abstract Number: B2002-03-2560R-016
Title: **Gated**-diode" configuration in **SOI MOSFET**'s: a sensitive tool for evaluating the quality and reliability of the buried **Si**/SiO/sub 2/ interface
Author(s): Xuejun Zhao; Salman, A.; Ioannou, D.E.; Jenkins, W.C.; Hughes, H.
Author Affiliation: Dept. of Electr. & Comput. Eng., George Mason Univ., Fairfax, VA, USA
Journal: AIP Conference Proceedings Conference Title: AIP Conf. Proc. (USA) no.550 p.226-30
Publisher: AIP,
Publication Date: 2001 Country of Publication: USA
CODEN: APCPCS ISSN: 0094-243X
SICI: 0094-243X(2001)550L.226:GDCM;1-2
Material Identity Number: A210-2001-005
U.S. Copyright Clearance Center Code: 0094-243X/01/$18.00
Conference Title: Characterization and Metrology for ULSI Technology 2000. International Conference
Conference Sponsor: NIST; Int. Semicond. Manuf. Technol.; Nat. Sci. Found.; American Vacuum Soc.; et al
Conference Date: 26-29 June 2000 Conference Location: Gaithersburg, MD, USA
Language: English
Abstract: A "**gated**-diode" configuration in **SOI MOSFET**'s is described, which is particularly suitable and easy to use for characterizing the **buried oxide** interface. This new approach becomes possible by taking advantage of the front **gate**, which is biased to inversion (NMOSFET's) or accumulation (BC-PMOSFET's) during the measurement. As a result, the **drain** merges with the inversion or accumulation layer and "extends" under the entire **gate**, forming a "horizontal" p-n junction with the channels. The **drain**-to-body diode is then forward-biased by a small voltage, and the back **gate** voltage is scanned such that it brings the back interface to depletion, a condition that is at the center of all **gated**-diode techniques and required to activate the interface states and start the recombination/generation processes. The midchannel interface state density is obtained from the peak of the measured current vs. back **gate** voltage curves, and by combining the measurements with 2D numerical simulations (e.g. a combination of SUPREM and PISCES), the interface state density profiles along the channel length near the source and **drain** can also be obtained.
Subfile: B

32/3,AB/2
DIALOG(R)File 2:INSPEC

6321942 INSPEC Abstract Number: B1999-09-2560R-069
Title: Threshold voltage model for deep-submicron fully depleted SOI MOSFETs with back **gate** substrate induced surface potential effects

Author(s): Imam, M.A.; Osman, M.A.; Osman, A.A.
Author Affiliation: Motorola Inc., Tempe, AZ, USA
Journal: Microelectronics Reliability vol.39, no.4 p.487-95
Publisher: Elsevier,
Publication Date: April 1999 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(199904)39:4L.487:TVMD;1-K
Material Identity Number: G489-1999-004
U.S. Copyright Clearance Center Code: 0026-2714/99/$20.00
Language: English
Abstract: A simple analytical threshold voltage model for short-channel fully depleted SOI MOSFETs has been derived. The model is based on the analytical solution of the two-dimensional potential distribution in the **silicon** film (front **silicon**), which is taken as the sum of the long-channel solution to the Poisson's equation and the short-channel solution to the Laplace equation, and the solution of the Poisson's equation in the **silicon** substrate (back **silicon**). The proposed model accounts for the effects of the back **gate** substrate induced surface potential at the **buried oxide**-substrate interface which contributed an additional 15-30% reduction in the threshold voltage for the devices used in this work. Conditions on the back **gate** supply voltage range are determined upon which the surface potential at the **buried oxide** -substrate interface is accumulated, depleted, or inverted. The short-channel associated **drain** induced barrier lowering effects are also included in the model. The model predications are in close agreement with PISCES simulation results. The equivalence between the present model and previously reported models is proven. The proposed model is suitable for use in circuit simulation tools such as Spice.
Subfile: B

32/3,AB/3
DIALOG(R)File 2:INSPEC

6262040 INSPEC Abstract Number: B1999-07-2560R-023
Title: An analytical symmetric double-**gate SOI MOSFET** model
Author(s): Hong-Kee Jiou; Sheng-Lyang Jang; Shau-Shen Liu
Author Affiliation: Kuang Wu Inst. of Technol. & Commerce, Taipei, Taiwan
Journal: International Journal of Electronics vol.86, no.6 p.671-83
Publisher: Taylor & Francis,
Publication Date: June 1999 Country of Publication: UK
CODEN: IJELA2 ISSN: 0020-7217
SICI: 0020-7217(199906)86:6L.671:ASDG;1-S
Material Identity Number: I097-1999-006
Language: English
Abstract: In this paper, we present a simple, complete and analytical **drain** current model for symmetric double-**gate** SOI MOSFETs. The model was developed using a quasi-two-dimensional Poisson's equation. The model, applicable to digital/analogue circuit simulation, contains the following advanced features: precise description of the sub-threshold, near threshold and above-threshold regions of operation by one single expression; single-piece **drain** current equation, smoothly continuous from the linear region to the saturation **region**, considering the **source/drain** resistance; inclusion of important short channel effects such as velocity saturation, **drain**-induced barrier lowering and channel length modulation; self-heating effect due to the low thermal

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conductivity of the **buried oxide** ; impact-ionization of MOS devices; and the parasitic BJT effect associated with **drain** breakdown.
Subfile: B

32/3,AB/4
DIALOG(R)File 2:INSPEC

5483246 INSPEC Abstract Number: B9703-2560R-013
Title: Hot-carrier-induced degradation in ultra-thin-film fully-depleted SOI MOSFETs
Author(s): Bin Yu; Zhi-Jian Ma; Zhang, G.; Chenming Hu
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: Solid-State Electronics vol.39, no.12 p.1791-4
Publisher: Elsevier,
Publication Date: Dec. 1996 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(199612)39:12L.1791:CIDU;1-G
Material Identity Number: S068-96012
U.S. Copyright Clearance Center Code: 0038-1101/96/$15.00+0.00
Language: English
Abstract: The charge-pumping measurement technique was successfully applied to submicron (L/sub eff/=0.35 mu m) n-MOSFETs on ultra-thin (50 nm) SOI film. The hot-carrier-induced degradation is studied by examining the damages to both **gate-oxide** and **buried-oxide** (BOX) interfaces. We found that when stressed at maximum substrate current, interface-trap generation is still the primary cause for hot-carrier-induced degradation. Even for ultra-thin-film SOI devices, the hot-carrier-induced damage is locally confined to the **gate**-oxide interface and only minor damage is observed at the **buried-oxide** interface. The **buried-oxide** interface charging contributes less than 5% of the overall **drain** current degradation.
Subfile: B

32/3,AB/5
DIALOG(R)File 2:INSPEC

5063167 INSPEC Abstract Number: B9511-1265D-017, C9511-5320G-013
Title: Low-voltage operation of a high-resistivity load SOI SRAM cell by reduced back-**gate**-bias effect
Author(s): Yamaguchi, Y.; Takahashi, J.; Yamaguchi, T.; Wada, T.; Iwamatsu, T.; Joachim, H.-O.; Inoue, Y.; Nishimura, T.; Tsubouchi, N.
Author Affiliation: ULSI Lab., Mitsubishi Electr. Corp., Itami, Japan
Journal: IEICE Transactions on Electronics vol.E78-C, no.7 p.812-17
Publication Date: July 1995 Country of Publication: Japan
CODEN: IELEEJ ISSN: 0916-8524
Language: English
Abstract: The stability of a high-resistivity load SRAM cell using thin-film **SOI MOSFET**'s was investigated as compared with bulk-**Si** MOSFET's. In **SOI MOSFET**'s back-**gate**-bias effect was suppressed by indirect application of back-**gate** bias to the channel region through the thick **buried oxide**. The V/sub t/

shifts were reduced to be 10% and 14% of that in bulk-**Si** MOSFET's in partially and fully depleted devices, respectively. The reduction of back-**gate** -bias effect provides improvement of "high" output voltage and gain in the enhancement-enhancement (EE) inverter in a high-resistivity load SRAM cell, thereby offering improved cell stability. It was demonstrated by using partially depleted SOI SRAM cells that non-destructive reading was obtained even at a low **drain** voltage of 1.4 V without **gate**-potential boost, which was much smaller than the operation limit in a bulk **Si** SRAM with the same patterns and dimensions used as a reference. This implies that SOI devices can also offer low-voltage operation even in TFT-load cells used in up-to-date high-density SRAM's. These results suggest that thin-film **SOI MOSFET** 's have a superior potential of low-voltage operation expected for further scaled devices and/or for portable systems in a forthcoming multimedia era.
Subfile: B C

32/3,AB/6
DIALOG(R)File 2:INSPEC

4817721 INSPEC Abstract Number: B9412-2560R-094
Title: Self-heating effects in **SOI MOSFET**'s operated at low temperature
Author(s): Jomaah, J.; Balestra, F.; Ghibaudo, G.
Author Affiliation: Lab. de Phys. des Composants a Semicond., CNRS, Grenoble, France
p.82-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xi+188 pp.
ISBN: 0 7803 1346 1
U.S. Copyright Clearance Center Code: 0 7803 1346 1/93/$3.00
Conference Title: Proceedings of 1993 IEEE International SOI Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-7 Oct. 1993 Conference Location: Palm Springs, CA, USA
Language: English
Abstract: In this work, self-heating effects are studied as a function of temperature. The electrical properties of fully depleted thin **Si** film N- and P-channel SIMOX MOSFETs are investigated between room and liquid helium temperatures. The P-and N-channel devices used in this study have been fabricated at LETI (Grenoble) with a conventionally-doped and a degenerately-doped LDD structures, respectively. The devices have an 11.5 nm **gate** oxide and a 380 nm **buried oxide** thicknesses. The article shows the **drain** current-**drain** voltage characteristics at 300 K for an N-channel SIMOX MOSFET fabricated with a degenerately doped LDD structure. The characteristics present a low negative differential resistance phenomenon for **gate** voltage up to 5 V. However, at 77 K, a strong negative differential resistance is observed for high **gate** voltages. The self heating effects are therefore significantly increased by reducing the temperature. This dependence is supposed to be due to the mobility variations and, also, the change with temperature of the threshold voltage.
Subfile: B

32/3,AB/7

DIALOG(R)File 2:INSPEC

04288029 INSPEC Abstract Number: B9301-2560R-017
Title: Threshold voltage and C-V characteristics of **SOI MOSFET**
's related to **Si** film thickness variation on SIMOX wafers
Author(s): Chen, J.; Solomon, R.; Chan, T.-Y.; Ko, P.K.; Hu, C.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., California Univ., Berkeley, CA, USA
Journal: IEEE Transactions on Electron Devices vol.39, no.10 p. 2346-53
Publication Date: Oct. 1992 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/92/$03.00
Language: English
Abstract: C-V characteristics of fully depleted SOI MOSFETs have been studied using a technique for measuring **silicon**-film thickness using a MOSFET. The technique is based on C-V measurements between the **gate** and source/**drain** at two different back-**gate** voltages, and only a large-area transistor is required. Using this technique, SOI film thickness mapping was made on a finished SIMOX wafer and a thickness variation of +or-150 AA was found. This thickness variation causes as much as a 100-mV variation in the device threshold voltage. The **silicon**-film thickness variation and threshold-voltage variation across a wafer shows a linear correlation dependence for a fully depleted device. C-V measurements of the back-**gate** device yield the **buried**-**oxide** thickness and parasitic capacitances. The effects of GIDL (**gate**-induced **drain** leakage) current on C-V characteristics are also discussed.
Subfile: B

32/3,AB/8
DIALOG(R)File 2:INSPEC

04038514 INSPEC Abstract Number: B9201-2560R-027
Title: Negative conductance model for short-channel **SOI MOSFET**
Author(s): Lai, J.C.; Fabian, T.; Liu, S.T.
Author Affiliation: Honeywell Solid State Electron. Center, Plymouth, MN, USA
Conference Title: 1990 IEEE SOS/SOI Technology Conference. (Cat. No.90CH2891-0) p.25-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA vi+178 pp.
ISBN: 0 87942 573 3
U.S. Copyright Clearance Center Code: CH2891-0/90/0000-0027$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1990 Conference Location: Key West, FL, USA
Language: English
Abstract: A short-channel SOI (**silicon** on insulator) n-channel MOSFET when source/**drain** junctions bottom out to the **buried** **oxide** may display a negative conductance in the output characteristics when the body tie is connected to the source. This phenomenon has been recently attributed to a temperature effect. However, the temperature effect is too small to account for the observation. Based on the theory of charge particle interaction in an electric field (between the channel electron flow and hole flow generated by impact ionization), a physical model is derived to account for the observation of the negative

conductance. The model is implemented in a modified SPICE program to facilitate the verification. The model fits to a short-channel SOI n-channel MOSFET made on a thin low-defect SIMOX material at V/sub GS/=5.0 V.
Subfile: B

32/3,AB/9
DIALOG(R)File 2:INSPEC

02948782 INSPEC Abstract Number: B87053728
Title: A novel self-aligned oxygen (SALOX) implanted **SOI** **MOSFET** device structure
Author(s): Tzeng, J.C.; Baerg, W.; Ting, C.; Siu, B.
Author Affiliation: Intel Corp., Santa Clara, CA, USA
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) vol.B21, no.2-4 p.112-15
Publication Date: March 1987 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
U.S. Copyright Clearance Center Code: 0168-583X/87/$03.50
Conference Title: Sixth International Conference on Ion Implantation Technology
Conference Sponsor: Appl. Mater.; Eaton Corp.; Tokyo Electron.; ASM America; Hitachi; et al
Conference Date: 28 July-1 Aug. 1986 Conference Location: Berkeley, CA, USA
Language: English
Abstract: The morphology of the novel self-aligned oxygen implanted SOI (SALOX **SOI**) **MOSFET** is studied. The channel **silicon** of SALOX SOI is confirmed to be undamaged single crystal **silicon** and connected with the substrate. **Buried oxide** formed by oxygen implantation in this SALOX SOI structure is shown by a cross section transmission electron micrograph (X-TEM) to be amorphous. The source/**drain** **silicon** on top of the **buried oxide** is single crystal, as shown by the transmission electron diffraction (TED) pattern. The **source/drain** **regions** are elevated due to the **buried** **oxide** volume expansion. A sharp **silicon**-**silicon** dioxide interface between the source/**drain** **silicon** and **buried** **oxide** is observed by Auger electron spectroscopy (AES). Well behaved n-MOS transistor current voltage characteristics are obtained and show no I-V kink.
Subfile: B

32/3,AB/10
DIALOG(R)File 2:INSPEC

02754939 INSPEC Abstract Number: B86063291
Title: An electrical method to measure SOI film thicknesses
Author(s): Whitfield, J.; Thomas, S.
Author Affiliation: Motorola Inc., Phoenix, AZ, USA
Journal: IEEE Electron Device Letters vol.EDL-7, no.6 p.347-9
Publication Date: June 1986 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/86/0600-0347$01.00
Language: English
Abstract: A method to nondestructively measure the **silicon** film

thickness and the **buried insulating** film thickness is presented. The method is based on a **silicon**-on-insulator (**SOI**) **MOSFET** , operating in the two regions where the threshold voltage depends on each of the film thicknesses. The method uses a feedback amplifier to hold the **drain** biases nearly constant while the body and/or the buried **gate** voltages are varied. Calculated threshold voltages from the top-**gate** voltages are used to calculate the film thicknesses. The method is illustrated on devices built in oxygen implanted substrates. The electrical measurements compare well with SEM image measurements.

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34/3,AB/1
DIALOG(R)File 2:INSPEC

6617573 INSPEC Abstract Number: B2000-07-2560R-091
Title: Simulated threshold voltage adjustment and drain current enhancement in novel striped-gate nondoped-channel fully depleted SOI-MOSFETs
Author(s): Koh, R.
Author Affiliation: Silicon Syst. Res. Labs., NEC Corp., Kanagawa, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.39, no.4B p.2229-35
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: April 2000 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(200004)39:4BL.2229:STVA;1-A
Material Identity Number: F221-2000-009
Conference Title: Solid State Devices and Materials. 1999 International Conference
Conference Date: 21-24 Sept. 1999 Conference Location: Tokyo, Japan
Language: English
Abstract: To enhance the performance of metal-oxide-**silicon** field-effect-transistors (MOSFETs), a new device having a **Silicon** -on-insulator (SOI) structure, called a striped-gate **SOI-MOSFET** , is proposed and its electrical characteristics are estimated by device simulation. The threshold voltage of this device is controlled by changing the length of a **metal layer** interposed in the gate electrode. A set of systematic device simulations reveals a type of two-dimensional effect in the gate electric field provides a continuous threshold voltage control for a non-doped channel **SOI-MOSFET** , and that the suppression of the channel doping provides a large drain current. A circuit simulation on a 2-input complementary-MOS (CMOS) NAND gate chain comprising the devices shows that the operation speed is enhanced by 46% compared with that of bulk MOSFETs, due to the device's large drain current and small parasitic capacitance.
Subfile: B

34/3,AB/2
DIALOG(R)File 2:INSPEC

6345081 INSPEC Abstract Number: B1999-10-2560R-058
Title: Physical and mathematical basis for the crucial technical shortcoming of the split C-V technique in thin-SOI MOSFETs
Author(s): Omura, Y.
Author Affiliation: Dept. of Electron. Eng., Kansai Univ., Osaka, Japan
Journal: Technology Reports of Kansai University no.41 p.69-74
Publisher: Kansai Univ,
Publication Date: March 1999 Country of Publication: Japan
CODEN: TRKUAW ISSN: 0453-2198
SICI: 0453-2198(199903)41L.69:PMBC;1-Z
Material Identity Number: T071-1999-001
Language: English

03/08/2002

Abstract: This paper describes the physical and mathematical basis of the crucial technical shortcoming of the conventional split C-V technique in thin-SOI MOSFETs. Mathematical expressions indicate that the conventional technique is only available for a very thick buried-oxide **layer** or a **metallic** back gate electrode.

Subfile: B